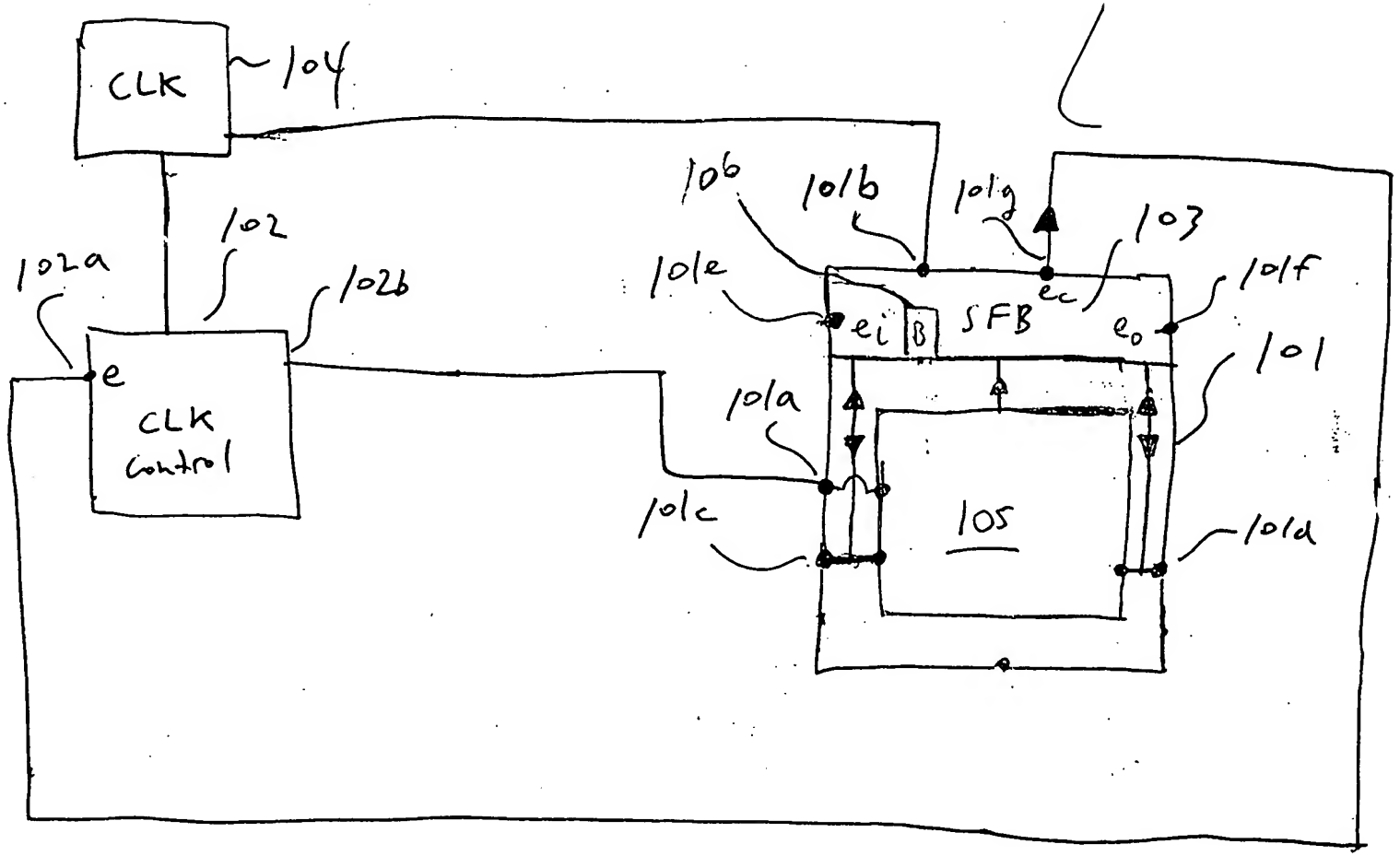
CLK
104
106
101b
101g
103
102
102a
102b
101e
101f
ei
B
SFB
eo
ec
e
CLK
Control
101
101a
101c
105
101d

FIG. 1

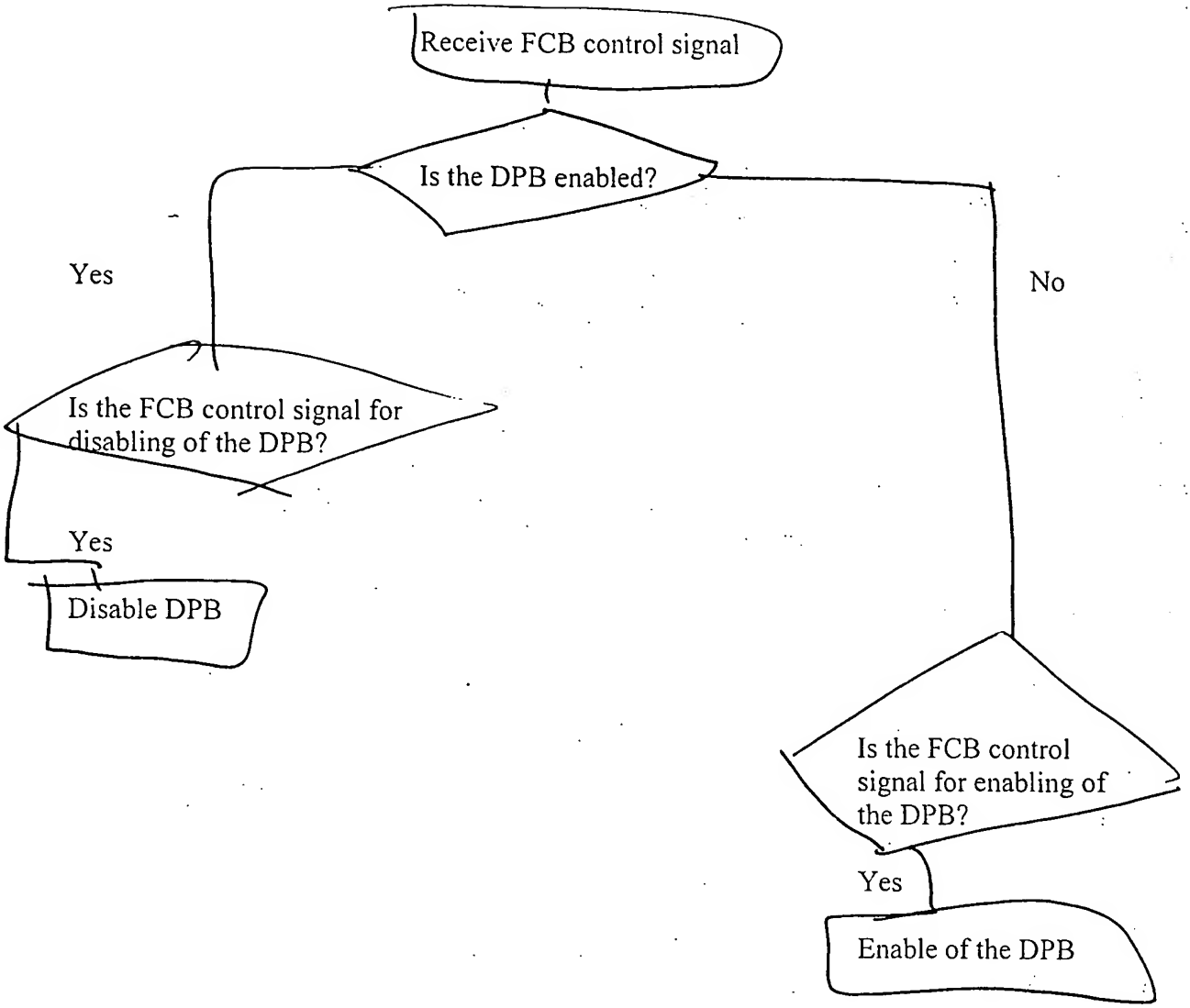
Receive FCB control signal
Is the DPB enabled?
Yes
No
Is the FCB control signal for disabling of the DPB?
Yes
Disable DPB
Is the FCB control signal for enabling of the DPB?
Yes
Enable of the DPB

FIG. 2a

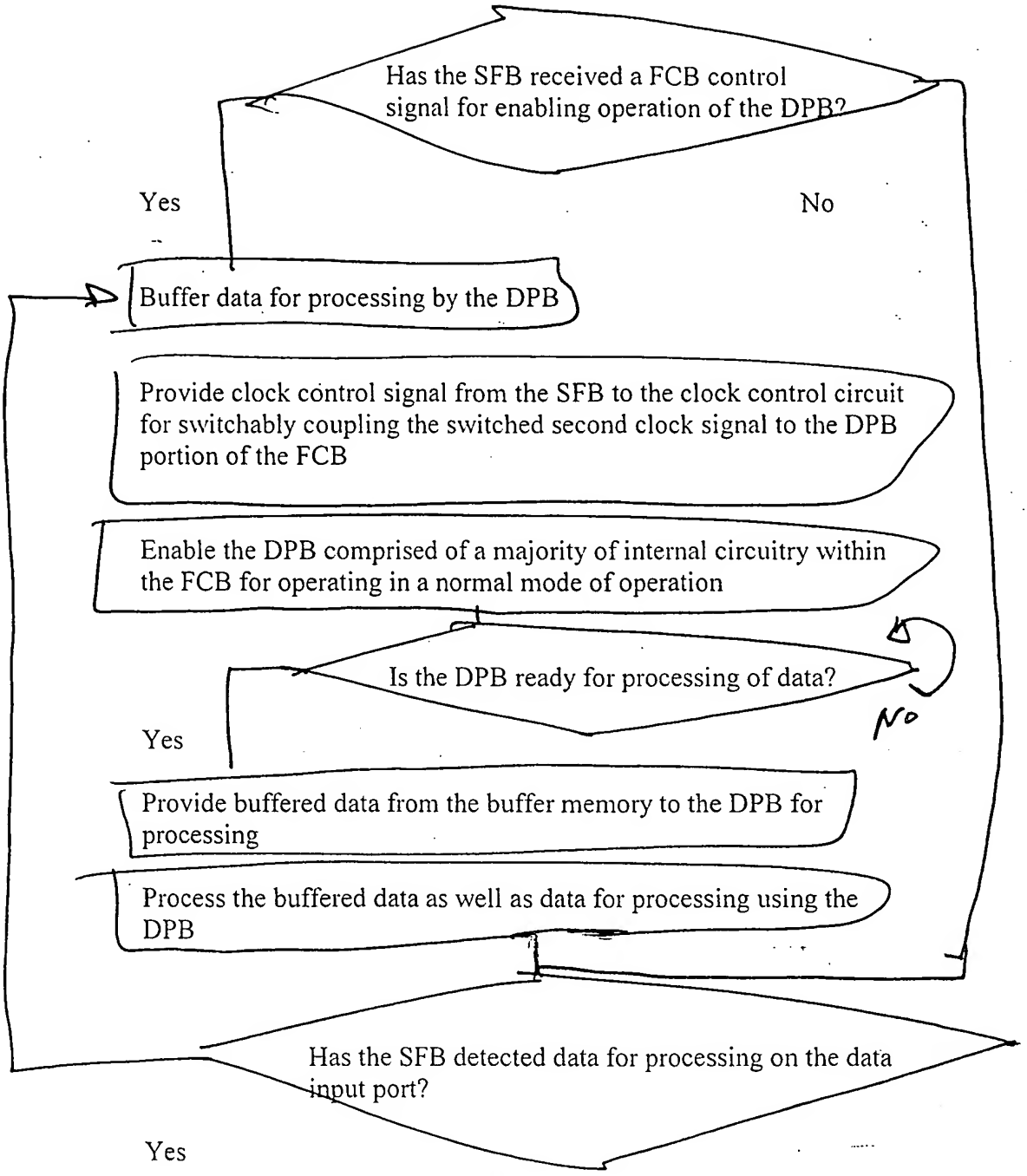
Has the SFB received a FCB control signal for enabling operation of the DPB?
Yes
No
Buffer data for processing by the DPB
Provide clock control signal from the SFB to the clock control circuit for switchably coupling the switched second clock signal to the DPB portion of the FCB
Enable the DPB comprised of a majority of internal circuitry within the FCB for operating in a normal mode of operation
Is the DPB ready for processing of data?
No
Yes
Provide buffered data from the buffer memory to the DPB for processing
Process the buffered data as well as data for processing using the DPB
Has the SFB detected data for processing on the data input port?
Yes

FIG. 26

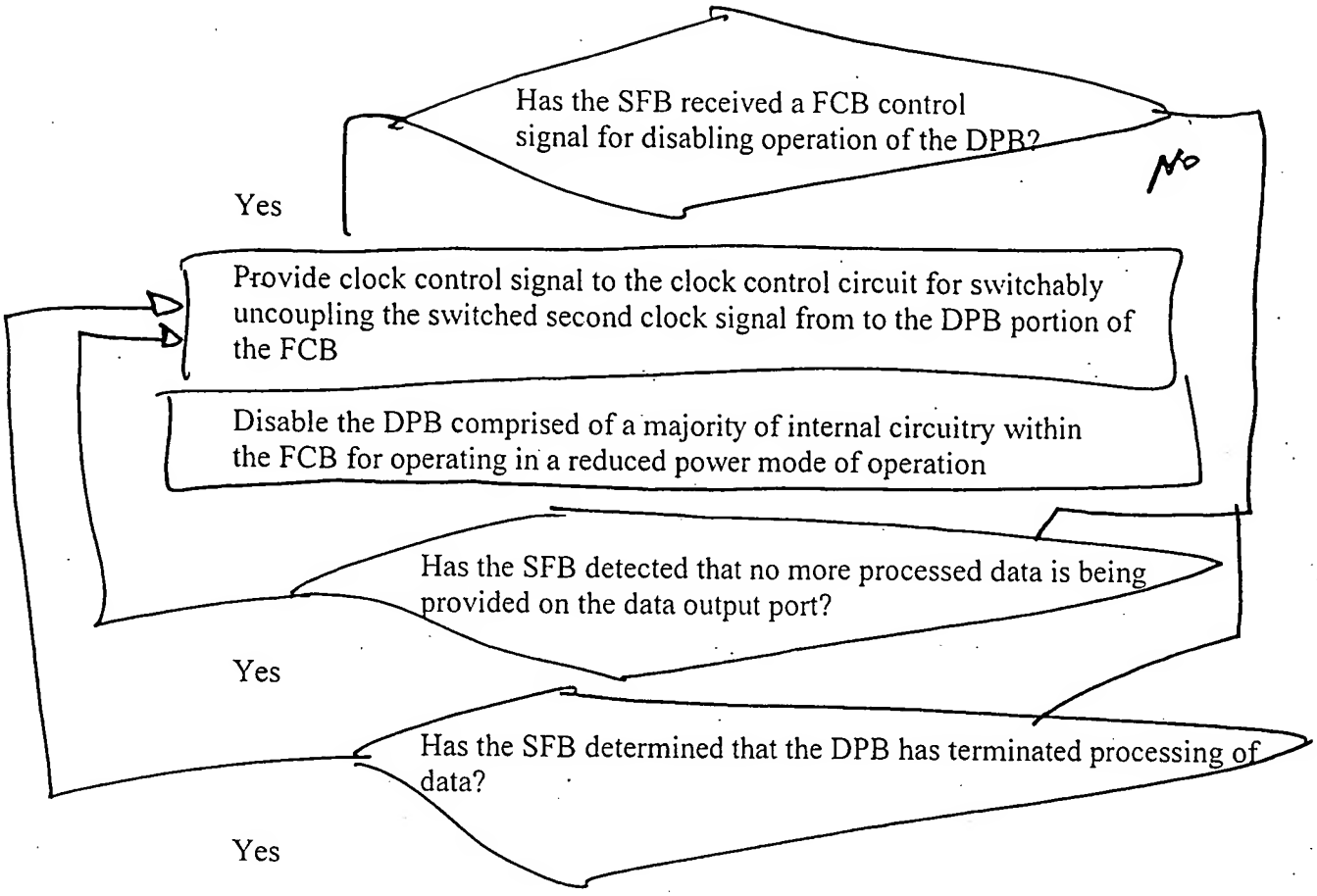
Has the SFB received a FCB control signal for disabling operation of the DPB?
No
Yes
Provide clock control signal to the clock control circuit for switchably uncoupling the switched second clock signal from to the DPB portion of the FCB
Disable the DPB comprised of a majority of internal circuitry within the FCB for operating in a reduced power mode of operation
Has the SFB detected that no more processed data is being provided on the data output port?
Yes
Has the SFB determined that the DPB has terminated processing of data?
Yes

FIG. 2c

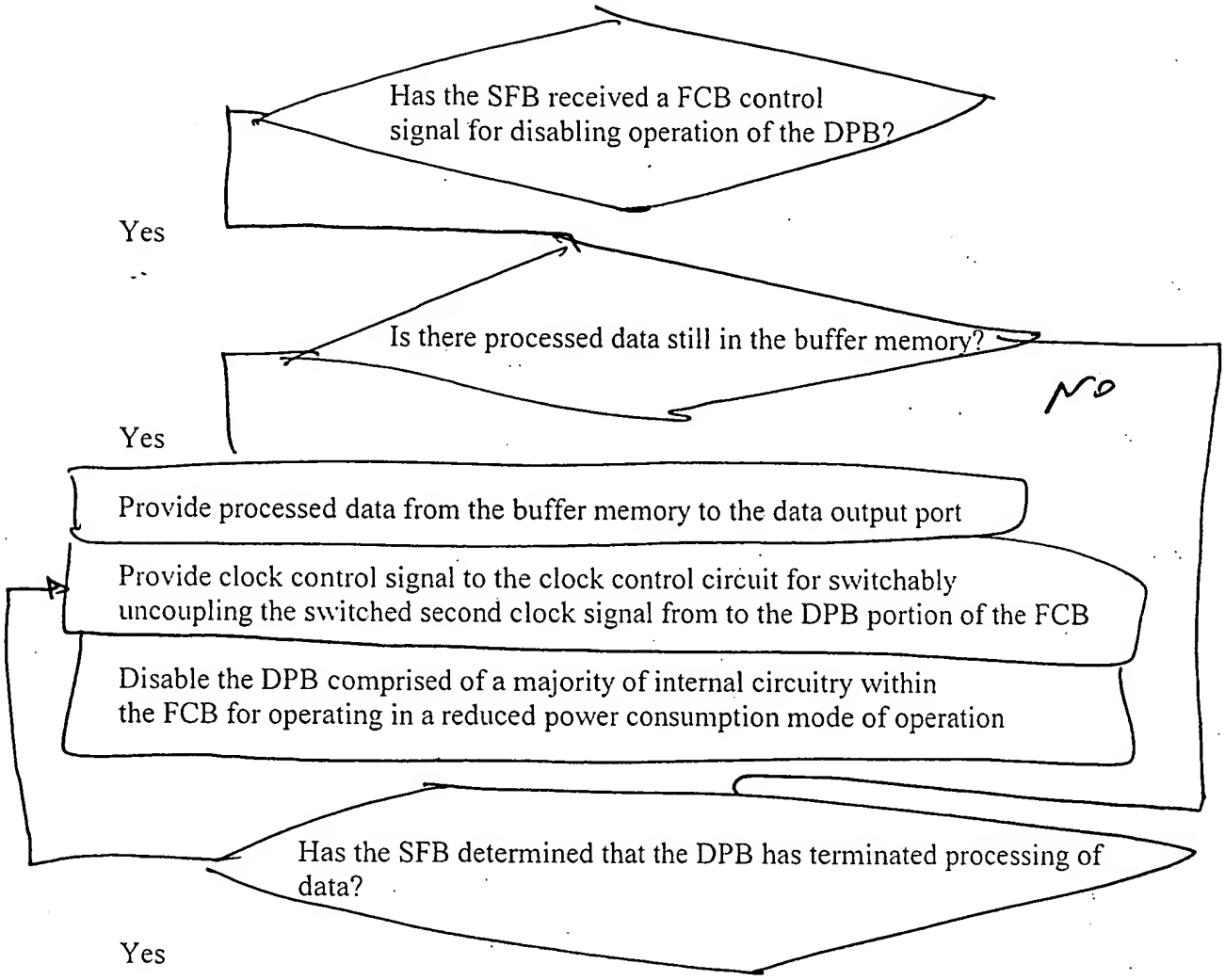
Has the SFB received a FCB control signal for disabling operation of the DPB?
Yes
Is there processed data still in the buffer memory?
No
Yes
Provide processed data from the buffer memory to the data output port
Provide clock control signal to the clock control circuit for switchably uncoupling the switched second clock signal from to the DPB portion of the FCB
Disable the DPB comprised of a majority of internal circuitry within the FCB for operating in a reduced power consumption mode of operation
Has the SFB determined that the DPB has terminated processing of data?
Yes

Fig. 2d

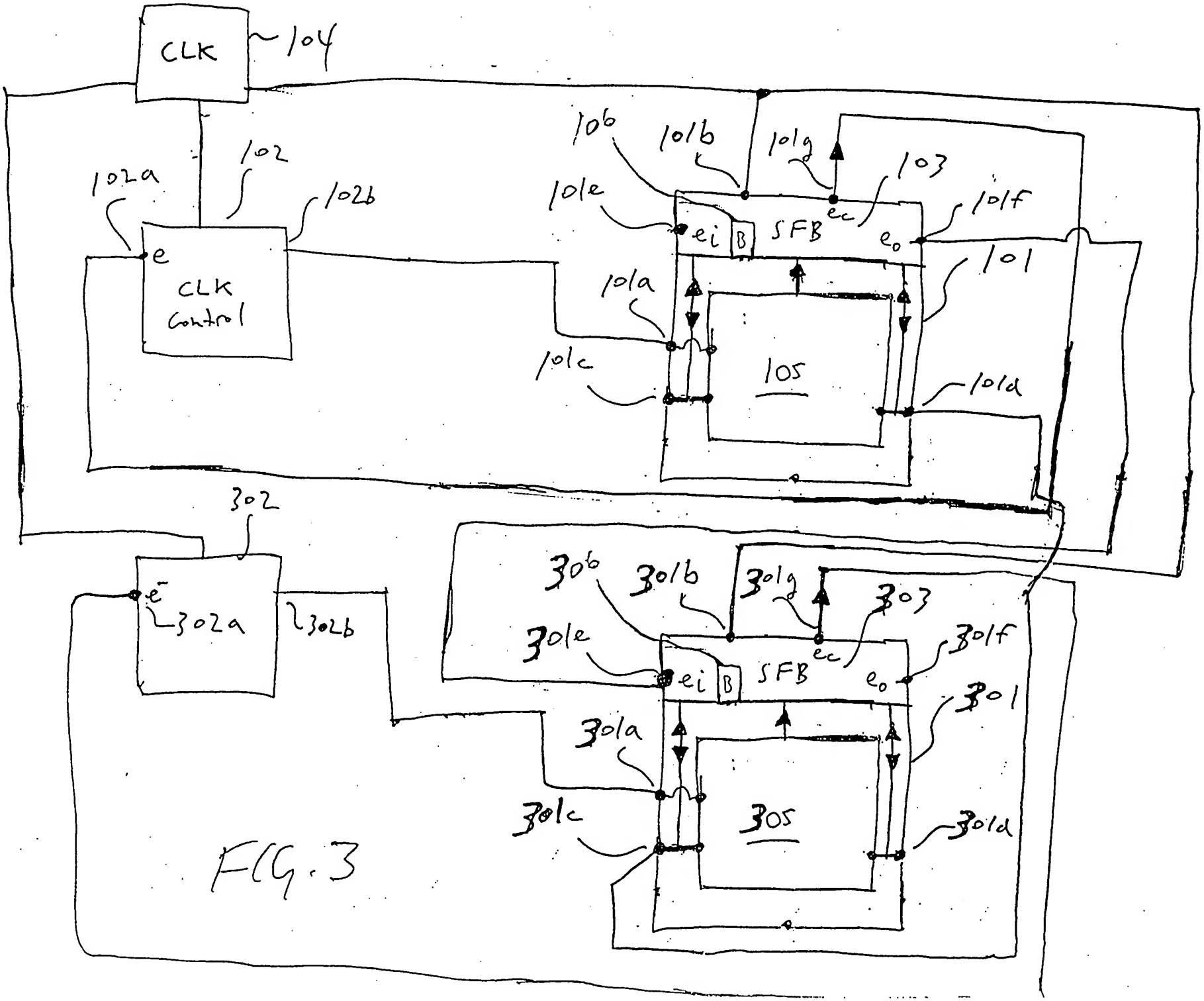
CLK
104
102
102a
102b
e
CLK
Control
106
101b
101g
103
101e
ei
B
SFB
ec
eo
101f
101
101a
101c
105
101d
302
302a
302b
306
301b
301g
303
301e
301f
301
301a
301c
305
301d

FIG. 3

Buffer data for processing provided on the data input port of the first FCB

Enable of the DPB portion of the first FCB using the SFB disposed in the first FCB

Provide a clock control signal from the first FCB to a first clock control circuit for switchably coupling of the second clock signal to the first FCB

Process data using the first FCB

Buffer processed data within the first FCB prior to providing this data to the second FCB

Provide a FCB control signal from the first FCB to the second FCB for enabling of the second FCB from the plurality of sequentially disposed FCBs

Terminate processing of data in the first FCB

Provide buffered data to the second FCB

Provide a clock control signal from the first FCB to the first clock control circuit for switchably uncoupling of the second clock signal to the first FCB

Disable the DPB portion of the first FCB using the SFB disposed in the first FCB so the first FCB operates in a reduced power consumption mode of operation

Process data using the second FCB.

Buffer processed data within the second FCB prior to providing this data to another FCB

Use the SFB disposed in the second FCB to determine when the second FCB has terminated processing of data

Provide a FCB control signal from the second FCB to another FCB for enabling of the another FCB from the plurality of sequentially disposed FCBs

Terminate processing of data in the second FCB

Provide buffered data to the another FCB

Provide a clock control signal from the second FCB to the second clock control circuit for switchably uncoupling of the third clock signal from the second FCB

Disable the DPB portion of the second FCB using the SFB disposed in the second FCB so the second FCB operates in a reduced power consumption mode of operation.

FIG. 4

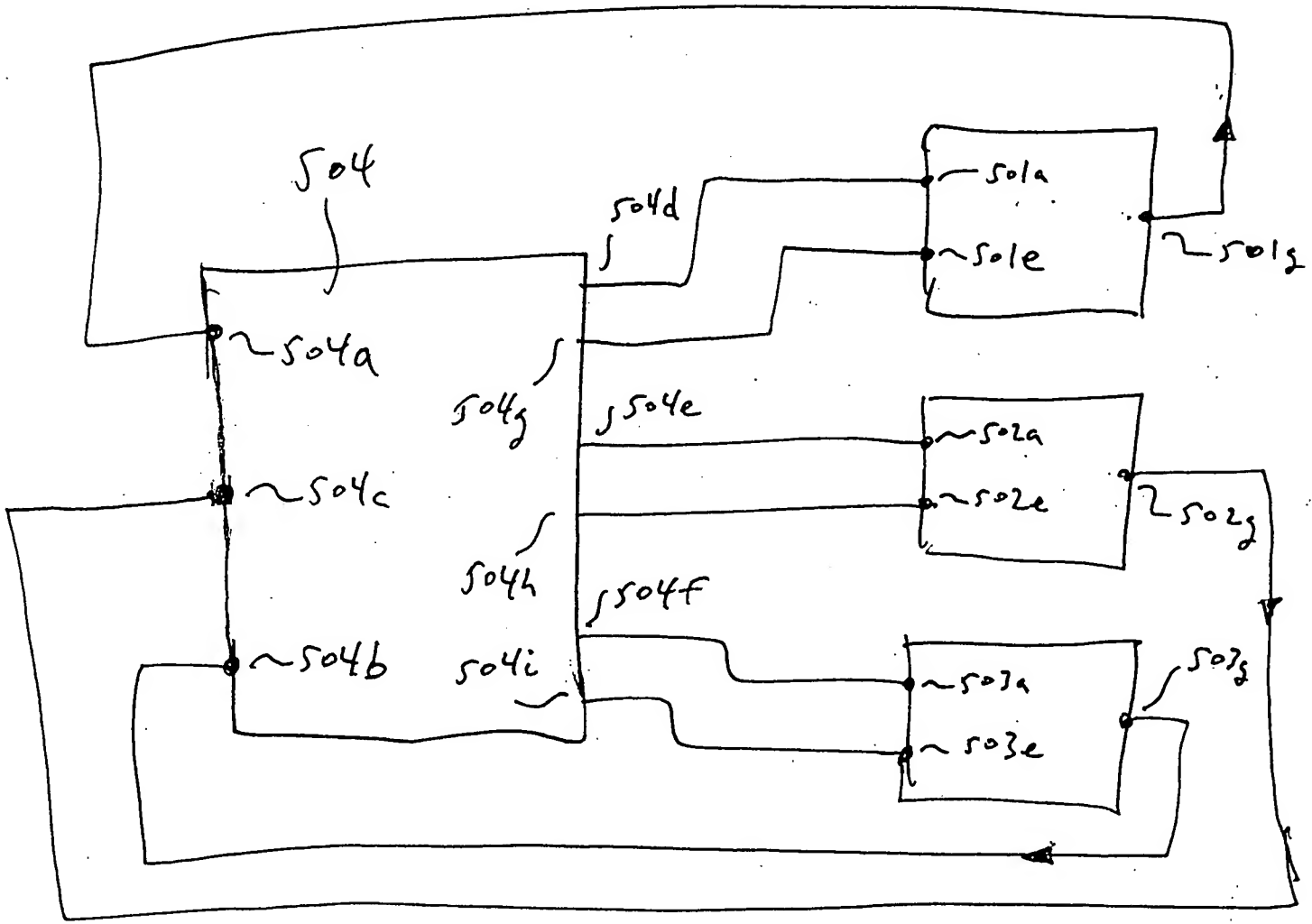
504
504d
501a
501e
501g
504a
504g
504e
502a
502e
502g
504c
504h
504f
504b
504i
503a
503g
503e

FIG. 5

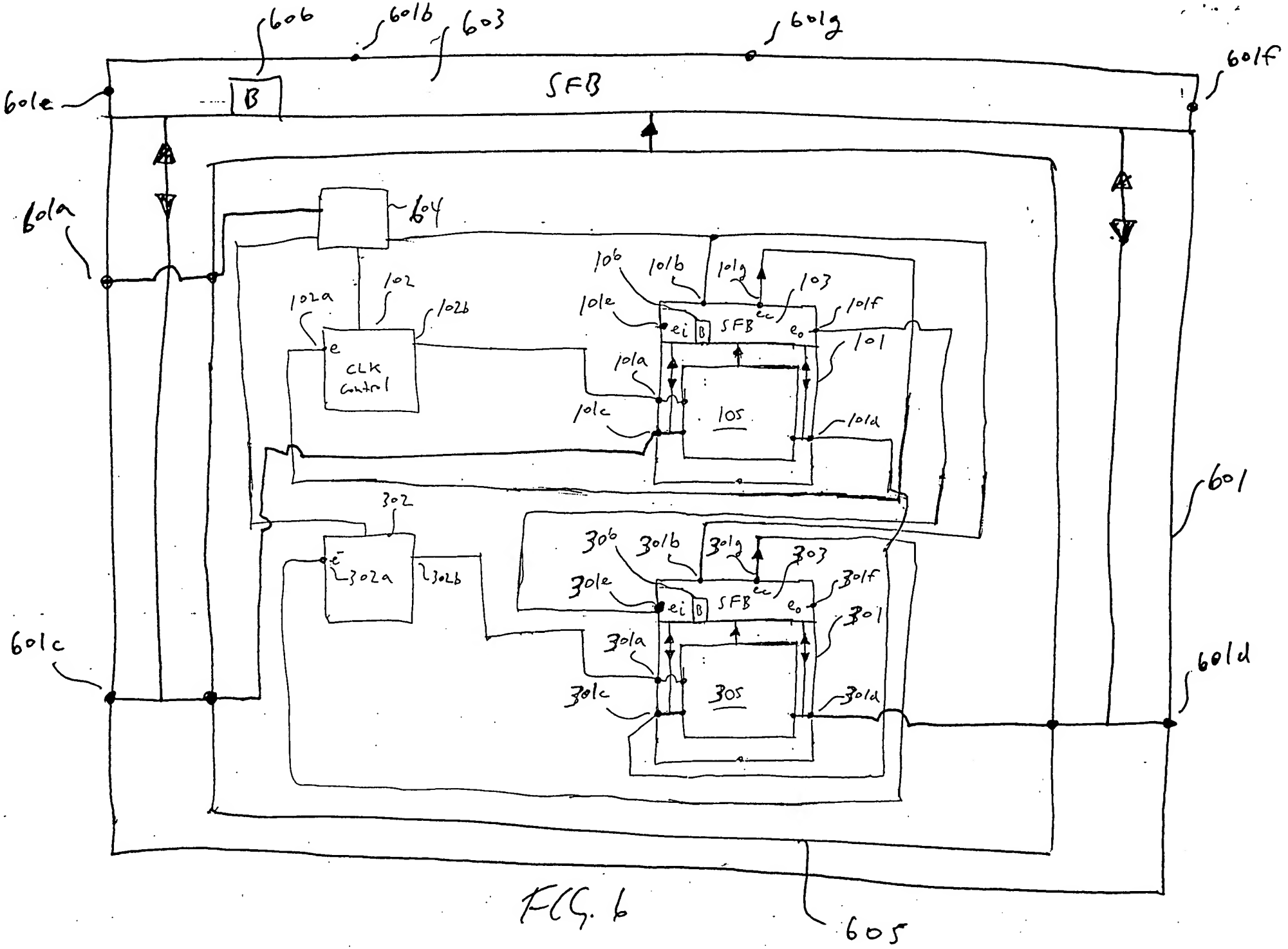
606
601b
603
601g
601f
601e
B
SFB
601a
604
106
101b
101g
107
101e
ei
B
SFB
eo
ec
101f
102
102a
102b
e
CLK
control
101
101a
101c
105
101d
601
302
302a
302b
306
301b
301g
303
301e
301f
301
301a
301c
305
301d
601c
601d
605

FIG. 6